



# UNITED STATES PATENT AND TRADEMARK OFFICE

*Handwritten signature*

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/007,468	11/07/2001	Shinichi Shimomaki	01727/LH	2858

1933 7590 01/14/2004

FRISHAUF, HOLTZ, GOODMAN & CHICK, PC  
767 THIRD AVENUE  
25TH FLOOR  
NEW YORK, NY 10017-2023

EXAMINER

JORGENSEN, LELAND R

ART UNIT PAPER NUMBER

2675

DATE MAILED: 01/14/2004

4

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/007,468

Applicant(s)

SHIMOMAKI, SHINICHI

Examiner

Leland R. Jorgensen

Art Unit

2675

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 07 November 2001.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1 - 19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 - 19 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. §§ 119 and 120**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All   b) ☐ Some \*   c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
- a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)                      4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)                      5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .                      6) ☐ Other: \_\_\_\_\_

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 2, and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Hirai, USPN 5,117,298.

### **Claims 1 and 12**

Hirai teaches a liquid crystal display device comprising a liquid crystal display panel 26 having a plurality of signal lines [data signal line 15] , a plurality of scanning lines [scan signal line 16], and a plurality of display pixels [liquid crystal element 14] arrayed in a matrix and provided respectively near cross-points between the signal lines and the scanning lines through switching elements. Hirai, col. 2, line 59 – col. 3, line 2; col. 8, lines 42 – 60; and figures 4 and 8. A driver [driving voltage generating part 23 with data driver part 25 and scan driver part 24] supplies the plurality of signal lines with a display signal in a field period, and which scans the plurality of scanning lines, to apply the display signal to the plurality of display pixels. Hirai, col. 8, lines 42 – 68; and figures 8 and 9. The driver applies a predetermined initialization signal

Art Unit: 2675

voltage  $[\pm(V_P - V_D)]$  to the display pixels, and thereafter applies the display signal [data signal] in at least one signal application period set within the field period. Hirai, col. 3, lines 3 – 29; col. 5, lines 33 – 49; col. 8, lines 11 – 32; and figures 5 and 7.

### **Claim 2**

Hirai adds wherein the liquid crystal display panel includes a plurality of pixel electrodes [lead electrode 3 and upper electrode 5 on the salient electrode 11] arrayed in a matrix through the switching elements, and common electrodes [upper transparent electrode 9] opposed to the pixel electrodes, and the display pixels comprise the pixel electrodes, the common electrodes, and liquid crystal [liquid crystal layer 10] sandwiched between the pixel electrodes and the common electrodes. Hirai, col. 2, lines 33 – 46; and figures 1 – 3.

3. Claims 1, 3, and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoon, USPN 6,005,542.

### **Claims 1 and 12**

Yoon teaches a liquid crystal display device comprising a liquid crystal display panel having a plurality of signal lines [data line], a plurality of scanning lines [gate line (e.g., a scanning line or a word line)], and a plurality of display pixels [pixel electrode  $C_{LC}$ ] arrayed in a matrix and provided respectively near cross-points between the signal lines and the scanning lines through switching elements. Yoon, col. 1, lines 15 – 36; and figures 1A and 1B. A driver [not shown] supplies the plurality of signal lines with a display signal in a field period, and which scans the plurality of scanning lines, to apply the display signal to the plurality of display pixels. Yoon, col. 2, lines 11 – 29; and figures 2 and 3. The driver applies a predetermined

Art Unit: 2675

initialization signal voltage [V<sub>gate</sub>] to the display pixels, and thereafter applies the display signal [V<sub>sig</sub>] in at least one signal application period set within the field period. Yoon, col. 2, lines 11 – 29; and figures 2 and 3.

### **Claim 3**

Yoon teaches that each of the switching elements of the liquid crystal display panel includes a thin film transistor. Yoon, col. 1, lines 9 – 25.

4. Claims 1 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Tomomura et al., USPN 6,362,803 B1.

### **Claims 1 and 12**

Tomomura teaches a liquid crystal display device comprising a liquid crystal display panel 10 having a plurality of signal lines [signal electrodes SEG<sub>i</sub> (i = 1, 2, 3, ..., m, ..., n)] , a plurality of scanning lines [signal electrodes COM<sub>i</sub> (i = 1, 2, 3, ..., m, ..., p)], and a plurality of display pixels arrayed in a matrix and provided respectively near cross-points between the signal lines and the scanning lines through switching elements. Tomomura, col. 5, lines 11 – 57; and figures 1 and 2. A driver [scanning side driver circuit 11A] supplies the plurality of signal lines with a display signal in a field period, and which scans the plurality of scanning lines, to apply the display signal to the plurality of display pixels. Tomomura, col. 5, lines 11 – 57; and figures 1 - 3. The driver applies a predetermined initialization signal voltage [correction pulse potential VC2 or VC4] to the display pixels, and thereafter applies the display signal in at least one signal application period set within the field period. Tomomura, col. 6, lines 16 – 51; and figures 4A – 4D.

5. Claims 1, 3 – 5, 7 - 14, and 16 - 19 are rejected under 35 U.S.C. 102(e) as being anticipated by McKnight, USPN 6,078,303.

**Claims 1 and 12**

McKnight teaches a liquid crystal display device comprising a liquid crystal display panel. It is inherent that such display have a plurality of signal lines, a plurality of scanning lines, and a plurality of display pixels arrayed in a matrix and provided respectively near cross-points between the signal lines and the scanning lines through switching elements. McKnight, col 6, line 53 – col. 7, line 20; and figures 7A & 7B. A driver [electrode control driver 110 and Pixel Driver Logic 102} supplies the plurality of signal lines with a display signal in a field period, and which scans the plurality of scanning lines, to apply the display signal to the plurality of display pixels. McKnight, col. 7, lines 21 – 59; and figure 2A. The driver applies a predetermined initialization signal voltage [Pulse 401] to the display pixels, and thereafter applies the display signal in at least one signal application period set within the field period. McKnight, col. 8, lines 7 – 56; col. 13, lines 28 – 58; and figures 2C and 7A.

**Claim 3**

McKnight teaches that each of the switching elements of the liquid crystal display panel includes a thin film transistor. McKnight, col. 2, lines 19 – 26; col. 12, lines 32 – 45; and figures 6A – 6D.

**Claims 4 and 13**

McKnight teaches that the driver applies the initialization signal voltage to the display pixels and thereafter applies the display signal after a predetermined hold time  $[t_0 \text{ to } t_1]$ , in the

Art Unit: 2675

signal application period in the field period, and the hold time is set to a time equal to or longer than a voltage-write response time [curve 161] of the display pixels. McKnight, col. 8, lines 7 – 66; and figures 2C and 2D.

#### **Claims 5 and 14**

McKnight teaches that the initialization signal voltage in the driver has a value equal to or higher than a maximum voltage value of the display signal. McKnight, col. 7, line 50 – col. 8, line 20; and figures 2B & 2C.

#### **Claims 7 and 16**

McKnight teaches that the application timing is set such that the driver applies the initialization signal voltage simultaneously to all the display pixels of the liquid crystal display panel, and thereafter applies the display signal to the display pixels connected to the scanning lines of the liquid crystal display panel, at a predetermined time interval, sequentially for every one of the scanning lines, in the signal application period in the field period. McKnight, col. 13, line 59 – col. 14, line 22; and figures 7A and 7B.

#### **Claims 8 and 17**

McKnight teaches that the driver provides three signal application periods in one field period. McKnight, col. 9, line 32 – col. 10, line 52; and figures 3A and 3B.

#### **Claims 9 and 18**

McKnight teaches that the display signal comprises first, second, and third color component signals, and the driver applies the initialization signal voltage and thereafter applies any one of the first, second, and third color component signals, to the display pixels connected to the scanning lines of the liquid crystal display panel, sequentially for every one of the scanning

Art Unit: 2675

lines, in each of the signal application periods of the field period. McKnight, col. 9, line 32 – col. 10, line 52; and figures 3A and 3B.

#### **Claims 10 and 19**

McKnight teaches that an illumination light source capable of controlling light emission color, the illumination light source being controlled to have light emission color corresponding to any one of the first, second, and third color component signals that is applied by the driver in each of the signal application period. McKnight, col. 9, line 32 – col. 10, line 52; and figures 3A and 3B.

#### **Claim 11**

McKnight teaches that the first color component signal is a red component signal, the second color component signal is a green component signal, and the first color component signal is a blue component signal. McKnight, col 1, lines 52 - 67.

6. Claims 1, 6, 12, and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Ono et al., USPN 5,790,089.

#### **Claims 1 and 12**

Ono teaches a liquid crystal display device comprising a liquid crystal display panel 100 having a plurality of signal lines [column electrodes  $X_1$  to  $X_M$ ], a plurality of scanning lines [row electrodes  $Y_1$  to  $Y_N$ ], and a plurality of display pixels [liquid crystal layer 102] arrayed in a matrix and provided respectively near cross-points between the signal lines and the scanning lines through switching elements [two-terminal type active element 103]. Ono, col. 1, lines 62 – col. 2, line 24; col. 11, lines 6 – 16; and figure 1. A driver supplies the plurality of signal lines



Art Unit: 2675

with a display signal in a field period, and which scans the plurality of scanning lines, to apply the display signal to the plurality of display pixels. Ono, col. 1, lines 62 – col. 2, line 24; col. 11, lines 6 – 16; and figure 1. The driver applies a predetermined initialization signal voltage  $[V_{msB}]$  to the display pixels, and thereafter applies the display signal [pulses  $2V_a$ ] in at least one signal application period set within the field period  $[Th]$ . Ono, col. 8, lines 15 – 53; and figure 11.

### **Claims 6 and 15**

Ono teaches that the driver applies the initialization signal voltage and the display signal to the display pixels connected to the scanning lines of the liquid crystal display panel, at a predetermined time interval, sequentially for every one of the scanning lines, in the signal application period in the field period, and the time interval is set to a value at which timings of applying the initialization signal voltage and the display signal to every of the display pixels connected to each of the scanning lines do not overlap each other. Ono, col. 8, lines 15 – 53; and figure 11.

### ***Conclusion***

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nagata et al., USPN 5,706,023, teaches a modulation signal.

Kusafaka et al., USPN 5,995,074, teaches a driving method having a pulse.

Nakajima et al., USPN 6,484,864 B1, teaches a driving method using a pulse.

Tanaka et al., JP 406175101 A, teaches a driving method for a ferroelectric liquid crystal.

Art Unit: 2675

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leland Jorgensen whose telephone number is 703-305-2650. The examiner can normally be reached on Monday through Friday, 7:00 a.m. through 3:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven J. Saras can be reached on 703-305-9720.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks  
Washington, D.C. 20231


**or faxed to:**

**(703) 872-9306**

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office, telephone number (703) 306-0377.

lrj



STEVEN SARAS  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600